REMARKS

Claims 1 - 4 and 7 – 24 were pending in the present application for patent as of the Office Action of January 12, 2006. In the Office Action of January 12, 2006, the Examiner objected to claim 9 as being dependent upon a rejected base claim, but would be allowable in rewritten in independent form, allowed claims 10 – 24, rejected claim 1 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent Number 5,835,754, Nakanishi, and rejected claims 2 - 8 under 35 U.S.C. 103(a) as being unpatentable over Nakanishi in view of U.S. Patent Number 6,057,998, Rupley, II et al. The examiner made the Office Action final.

Claim 1 was rejected under 35 U.S.C. 102(b) as being anticipated by Nakanishi. The examiner cited several portions of Nakanishi to support the examiner's position. The applicants continue to assert that claim 1 is allowable over Nakanishi as originally filed. In addition to the applicants' previous comments, the applicants would like to add the following.

Nakanishi does not show or suggest a method for allocating entries in a BTB as claimed in original claim 1. The examiner cites the abstract of Nakanishi to show, at least in part, the claim 1 limitations of (1) "determining if the branch target address location can be obtained without causing a further stall condition in the pipelined data processing system" and (2) "selectively allocating a BTB entry based on the determination". However, the abstract of Nakanishi only outlines what is included in a BTB entry (e.g. an offset), what is outputted from the BTB entry, and how the BTB entry is used. The abstract does not show or suggest allocating BTB entry as claimed in claim 1.

The examiner cited Nakanishi at column 1, lines 12 – 15 as disclosing the limitations labeled (1) and (2) above. However, Nakanishi only discloses at column 1, lines 12 – 15 that it is important that a superscalar processor not be stalled.

The examiner cited Nakanishi at column 1, line 54 to column 2, line 7 as disclosing the limitations (1) and (2) of claim 1 regarding how a BTB entry is allocated. However, Nakanishi at column 1, line 54 to column 2, line 7 only discloses how the tags are read out of the BTB, and does not disclose the limitations (1) and (2) of claim 1.

The examiner cited Nakanishi at column 2, lines 55 – 67 as disclosing the limitations (1) and (2) of claim 1 regarding how a BTB entry is allocated. Nakanishi at column 2, lines 55 – 67 discloses that a branch is predicted as not taken when a tag is not found and the next sequential

instruction address is obtained. This cited section of Nakanishi does not discuss how a BTB entry is allocated.

The examiner cited Nakanishi at column 3, lines 29 – 33 and column 3, lines 48 – 55 as disclosing the limitations (1) and (2) of claim 1. Column 3, lines 29 – 33 discloses that the BTB cannot be accessed until after a branch instruction is recognized and decoded. Column 3, lines 48 – 55 discloses that in the case of superscalar processor, the BTB is accessed simultaneously with the fetch of the instruction, and if the instruction is not found in the BTB it is predicted to be not taken. Neither section of Nakanishi discloses how a BTB entry is allocated.

The examiner cited Nakanishi at column 6, lines 13 – 19 as disclosing the limitations (1) and (2) of claim 1. Column 6, lines 13 – 19 discloses how a program counter value and offsets are used. This cited section of Nakanishi does not discuss how a BTB entry is allocated.

The examiner cited Nakanishi at column 8, lines 19 – 21 and column 8, lines 35 – 54 as disclosing the limitations (1) and (2) of claim 1. These cited sections discuss the contents of a BTB entry. They do not disclose how a BTB entry is allocated.

The examiner cited Nakanishi at column 10, lines 1 – 16 as disclosing the limitations (1) and (2) of claim 1. This section of Nakanishi discloses that a BTB entry is entered based on whether the branch is taken or not taken. However, this is the same determination disclosed in the background section of the present application at page 2, lines 9 – 15, and is not the same as "determining if the branch target address location can be obtained without causing a further stall condition in the pipelined data processing system" as claimed in claim 1.

The examiner cites column 1, lines 23 – 29 of Nakanishi as implying that performing a branch prediction simultaneously with instruction fetch "eliminates the wait that branch instructions would otherwise have created". However, the applicants respectfully disagree. The next paragraph of Nakanishi (column 1, lines 30 – 42) states that if the branch prediction is wrong, the processor suffers from a delay (stall). Also, the applicants respectfully assert that a BTB entry is not necessarily filled at the time branch prediction is occurring. For example, Nakanishi at column 2, lines 9 and 10 disclose that "Entry of information into the BTB 31 is performed during execution of the branch instruction". Also, column 2, lines 19 – 21 states that "In some cases, the entry of information into the BTB 31 is not performed when the branch is not taken". In both of these cases, a stall condition may have been encountered before the execution of the branch instruction. Nakanishi also discloses at column 9, lines 63 - 65 that entry into the

BTB is performed while the branch instruction is executed, such as discussed in the background section of the present application at page 2, lines 9 – 15. In Nakanishi, information is recorded in the BTB whether the branch is taken or not taken (column 2, lines 10 - 14). Nakanishi does not determine if the branch target address location can be obtained without causing a further stall condition in the pipelined data processing system. Also, Nakanishi does not selectively allocate a BTB entry based on the determination. Therefore, the applicants believe that claim 1, as originally filed is allowable over Nakanishi.

The applicants do not assert that the method of claim 1 prevents stalls, but that the method of claim 1 is more efficient and more cost effective for low cost systems. The prior art, such as disclosed by Nakanishi and the background section of the present application, simply fills an entry of a BTB based on whether a branch was previously taken or not taken in order to reduce the likelihood of a stall condition the next time the branch instruction is encountered. The method of claim 1, on the other hand, looks at whether or not the branch target address location can be obtained without causing a further stall condition, and then allocating a BTB entry based on the determination. The claim 1 method for allocating a BTB entry is different than the method disclosed by Nakanishi, even though their goals of avoiding stalls is the same. Nakanishi does not base allocating a BTB entry on whether or not the branch target address location can be obtained without causing a further stall condition. Nakanishi just waits until a branch is determined to be taken or not taken before loading a BTB entry. Therefore, the applicants believe that claim 1, as originally filed, is allowable over Nakanishi.

Claims 2 - 8 were rejected under 35 U.S.C. 103(a) as being unpatentable over Nakanishi in view of Rupley, II et al. The applicants believe that claims 2 - 8 are allowable over Nakanishi in view of Rupley, II et al. for at least the reasons given above for claim 1.

The Office Action contains numerous statements characterizing the claims, the Specification, and the prior art. Regardless of whether such statements are addressed by Applicants, Applicants refuse to subscribe to any of these statements, unless expressly indicated by Applicants.

No amendment made was related to the statutory requirements of patentability unless expressly stated herein. No amendment made was for the purpose of narrowing the scope of any claim, unless the applicants have argued herein that such amendment was made to distinguish over a particular reference or combination of references.

Believing to have responded to each and every rejection contained in the Office Action mailed January 12, 2006, the applicants respectfully request the reconsideration and allowance of claims 1 - 4 and 7 - 24; thereby placing the application in condition for allowance.

Respectfully submitted,

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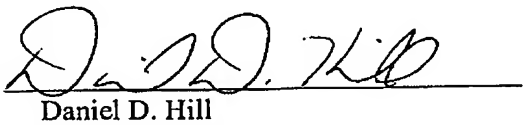
By: 

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